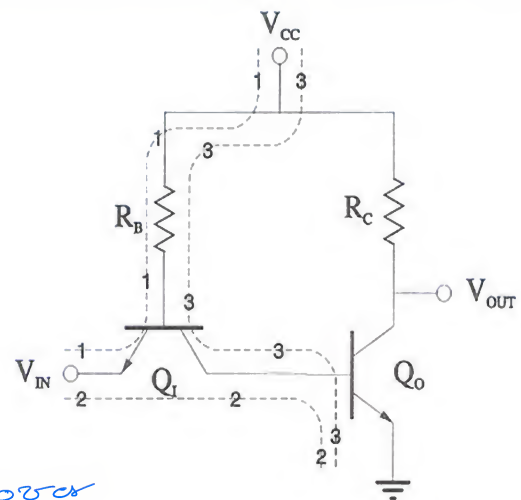


Chapter 7: Transistor Transistor Logic (TTL)

- * The usage of diodes in DTL is replaced with transistors (BJTs) in TTL. The resulting TTL circuits provide increased fan-out, improved transient response & a reduction in chip area required.
- * The 74X00 series are adequate for most commercial applications (0° to 70°)
- * The 54X00 series primarily used for military applications (-55° to 125°)
- * The main improvement in TTL design over DTL is the inclusion of active pull-up sub-circuit. This results in faster charging of the equivalent output capacitance.

Basic TTL Inverter

- * The input & level-shifting diodes of the basic DTL inverter have been replaced with a single BJT Q_1 at the input
- * The JBE of Q_1 replaces the DTL input diode
- * The JBC of Q_1 replaces the DTL level shifting diode. & the base of the BJT acts as a common region.
- * The advantage of the input BJT over the diodes is two-fold:
 1. The BJT requires less silicon surface area than the two diodes
 2. The propagation delay time is improved by an order of magnitude.



Output high voltage $\equiv V_{OH}$

- * For V_{IN} low the JBE of the input BJT Q_1 is Forward-biased.

$$I_{B,1} = \frac{V_{CC} - V_{BE,1} - V_{IN}}{R_B}$$

- * The magnitude of $I_{B,1}$ is in milliamps range for typical values of R_B so Q_1 operates in saturation for V_{IN} low

$$V_{BE,0} = V_{IN} + V_{CE,1}(\text{sat})$$

* It's clear that Q_0 is cutoff for low V_{in}

$$V_{out} = V_{cc} = V_{OH}$$

Input low voltage $\equiv V_{IL}$

* As V_{in} increased Q_0 turns on when V_{in} reaches

$$V_{in} = V_{BE,0}(FA) - V_{CE,1}(sat) = V_{IL}$$

* with further increase of V_{in} the output voltage begins to reduce until Q_0 saturates.

Output low voltage $\equiv V_{OL}$

* As V_{in} is increased further the output voltage reaches its minimum which is $V_{CE,0}(sat)$ and

$$V_{OL} = V_{CE,0}(sat)$$

Input high voltage $\equiv V_{IH}$

* For Q_0 just saturated

$$V_{in} = V_{BE,0}(sat) - V_{CE,1}(sat) = V_{IH}$$

* Q_0 remains saturated for values of V_{in} higher than V_{IH}

* As V_{in} is increased further, the J_{BE} of Q_1 eventually becomes reverse biased

$$V_{BC,1} = (V_{cc} - I_{B,1}R_b) - V_{BE,0}(sat)$$

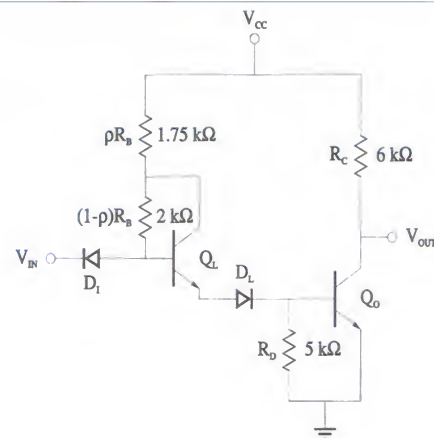
* J_{BC} of Q_1 is forward biased, therefore for high inputs Q_1 operates in the RA mode.

Comparison of stored-charge removal from DTL & TTL

* For DTL an additional resistor was added to the base of Q_0 to remove stored charge from the base when undergoing a transition from saturation to cutoff

* the initial current (upon switching) for stored charge removal is

$$I_{SCR} = I_{RD} = \frac{V_{BE,0}(sat)}{R_D}$$



*For the basic TTL R_D is unnecessary because Q_1 provides a low resistance path for charge removal

*When V_{in} is switched from high to low V_{C1} is still at

$$V_{C1} = V_{BE1}(sat)$$

& the input voltage to Q_1 , V_{E1} is switched to

$$V_{E1} = V_{OL} = V_{CE1}(sat)$$

*Since the JBC of Q_1 is now forward biased

$$V_{B1} = V_{E1} + V_{BE1}(FA) = V_{CE}(sat) + V_{BE}(FA)$$

$$V_{BC1} = V_{B1} - V_{C1} = V_{CE}(sat) + V_{BE}(FA) - V_{BE}(sat)$$

*While the JBC of Q_1 is forward biased it is insufficient to saturate Q_1 , & Q_1 therefore operates in the FA mode. the resulting collector current of Q_1 is

$$\begin{aligned} I_{C1} &= \beta_F I_{B1} = \beta_F \frac{V_{CC} - V_{B1}}{R_B} \\ &= \beta_F \frac{V_{CC} - V_{BE}(FA) - V_{CE}(sat)}{R_B} = -I_{B0} \end{aligned}$$

*which provides an enormous initial current (upon switching) for stored charge removal from the base of Q_0 . This in turn improves propagation delay time by an equivalent factor.

Example 7.1 Stored Charge Removal Comparison

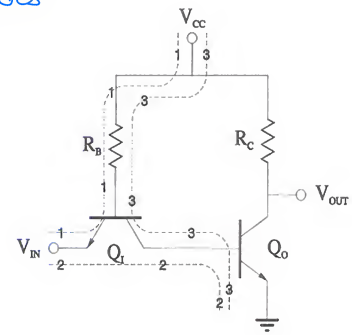
Calculate the factor of improvement for stored charge removal for TTL over DTL. Let $V_{CC} = 5$ V, $R_B = 2$ k Ω , and $R_D = 5$ k Ω . Use $\beta_F = 50$, $V_{BE}(FA) = 0.7$ V, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ V for the BJT.

$$I_{RD} = \frac{V_{BE}(sat)}{R_D} = \frac{0.8}{5k} = 160 \mu A$$

$$I_{B0} = \beta_F \frac{V_{CC} - V_{BE}(FA) - V_{CE}(sat)}{R_B} = (50) \frac{5 - 0.7 - 0.2}{2k} = 102.5 \mu A$$

the factor of improvement is therefore

$$\frac{102.5 \mu A}{160 \mu A} = 640.6$$



Basic TTL NAND gate & the multiple-emitter BJT

"The TTL logic family provides the logical NAND operation"

This is similarity between DTL & TTL

* A separate BJT could be used for each output with coupled bases & coupled collectors. However a unique alternative is to make use of the multiple-emitter BJT

* Any input low

If any input is low the corresponding J_{BE} junction is forward biased allowing a large current to flow in R_B & forcing Q_I into saturation. Q_O will be cutoff since

$$V_{BE,O} = V_{IN}(\text{low}) + V_{CE,I}(\text{sat}) < V_{BE}(\text{FA})$$

and thus $V_{OUT} = V_{CC} = V_{OH}$

* All inputs high

all J_{BE} 's of Q_I are reverse biased with J_{BC} forward biased, thus Q_I operating in RA mode. with Q_I providing a large current to the base of Q_O , Q_O is in saturation.

$$V_{OUT} = V_{CE,O}(\text{sat}) = V_{OL}$$

Therefore the basic TTL multiple-emitter BJT gate provides the NAND operation.

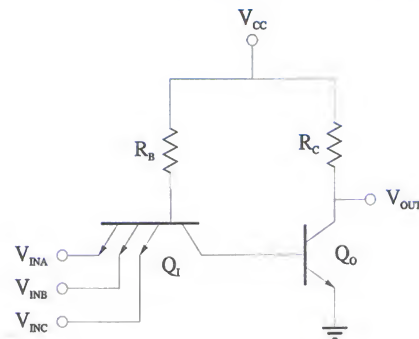


FIGURE 7.2 Basic TTL NAND Gate with Multi-emitter BJT Input Stage

Standard TTL NAND gate with totem pole output

* The stacking of two BJTs, a resistor and a diode in the output branch is called a "totem pole output".

Comparison of load capacitance charging for basic TTL & TTL with totem pole output

* The addition of R_{CP} & Q_P to output high driver portion of the circuit provides active pull-up. thus a large current is available for charging the equivalent load capacitance when the output switches from low to high

* For the basic TTL gate the equivalent load capacitance charges directly through R_C

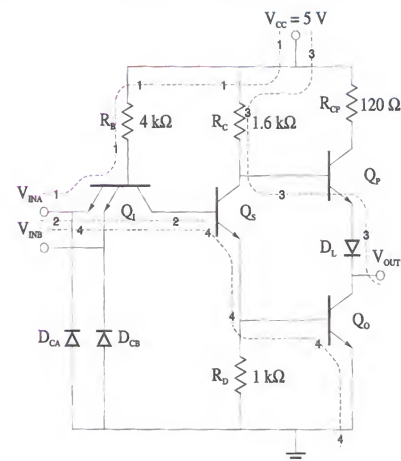


FIGURE 7.3 Standard 5400/7400 Series TTL NAND Gate with Totem-pole Output

resulting in a rise time constant given by

$$T_{\text{pull-up (passive)}} = R_C C_{EQ}$$

with initial current given by

$$I_{\text{pull-up (passive)}} = \frac{V_{CC} - V_{CE,sat}}{R_C}$$

* For the TTL with active pull-up the equivalent load capacitance charges through R_{CP} , giving

$$T_{\text{pull-up (active)}} = R_{CP} C_{EQ}$$

where R_{CP} is typically a tenth of R_C . the initial current for the active pull-up circuit can be found following the totem pole output branch

$$\begin{aligned} I_{\text{pull-up (active)}} &= \frac{V_{CC} - V_{CE,P(sat)} - V_{D,L(on)} - V_{CE,O(sat)}}{R_{CP}} \\ &= \frac{V_{CC} - 2V_{CE(sat)} - V_{D(on)}}{R_{CP}} \end{aligned}$$

which is much larger than $I_{\text{pull-up (passive)}}$ because $R_{CP} \ll R_C$. therefore TTL gates with active pull-up have a much smaller rise time constant & much larger initial current than the basic TTL gates.

Other additional elements

* Q_S provides base driving current to Q_O to ensure saturation

* Along with R_C & D_L , Q_S also provides logic inversion to Q_P in the following manner. when Q_O is in saturation Q_S is in saturation & Q_P is off since

$$V_{B,P} = V_{BE,O(sat)} + V_{CE,S(sat)}$$

with

$$V_{E,P} = V_{CE,O(sat)} + V_{D,L(on)}$$

$$V_{BE,P} = V_{BE(sat)} - V_{D(on)} < V_{BE(FA)}$$

* Q_P & Q_O are never on simultaneously

* the input BJT Q_I aids in the pull down of Q_S

TABLE 7.1 Purpose of Each Element for a Series 5400/7400 Standard TTL Gate

Element	Purpose
Q_I	Multi-emitter input BJT, base-collector level shifting of transition width, pull-down of Q_S
R_B	Limits I_{IL}
Q_S	Drive splitter, provides base driving current to Q_{O1} , base-emitter level shifting for shift of transition width, pull-down of Q_P
R_C	Along with Q_S provides logic inversion to output-high driver
Q_O	Output inverting BJT, output low driver for current sourcing pull-down
D_L	Diode level shifting between V_{CC} and output
R_D	Provides discharge path for saturation stored charge of Q_O
Q_P	Provides active current-sourcing pull-up
R_{CP}	Part of active pull-up and limits current spikes during output high-to-low transitions
D_{C1}, D_{C2}	Input clamping diodes to limit the negative swing of the inputs to one diode drop below ground

* R_D is necessary to remove stored charge from the base of Q_0 since I_{C1} no longer directly sinks Q_0 . For standard TTL this is not since Q_0 for TTL does not as severe as in DTL become heavily saturated

Standard TTL VTC

* To determine the VTC of the standard TTL we consider the two inputs connected together with

$$V_{IN1} = V_{IN2} = V_{IN}$$

Output high voltage $\equiv V_{OH}$

* For V_{IN} low a large current flows into the base of Q_1

$$I_{B1} = \frac{V_{CC} - V_{BE1} - V_{IN}(\text{low})}{R_B}$$

* But for I_{C1} is limited to leakage current of Q_3 (which will momentarily be proven to be cutoff for low V_{IN})

$$I_{C1} = -I_{B3}(\text{leakage}) \ll \beta_F I_{B1}$$

Under these conditions $I_{C1} \ll I_{B1}$

And Q_1 is saturated

$$V_{B1} = V_{IN} + V_{CE1}(\text{sat}) < V_{BE}(\text{FA})$$

Hence, Q_3 & therefore Q_0 are cutoff for

$$V_{IN} < V_{BE1}(\text{FA}) - V_{CE1}(\text{sat})$$

$$I_{RC} = I_{C3} = 0, \text{ neglecting } I_{B3} \text{ \& } V_{BP} = V_{CC}$$

Thus, the JBE of Q_p & D_L will be forward biased

$$V_{out} = V_{CC} - V_{BE,p}(\text{FA}) - V_{D_L}(\text{on})$$

$$= V_{CC} - V_{BE}(\text{FA}) - V_D(\text{on}) = V_{OH}$$

V_{OH} is reached when the load is charged with Q_p & Q_s at the edge of conduction (EOC).

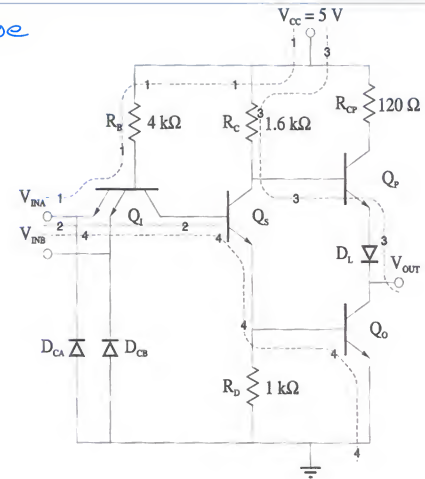


FIGURE 7.3 Standard 5400/7400 Series TTL NAND Gate with Totem-pole Output

Input low voltage $\equiv V_{IL}$

* As V_{IN} is increased & $V_{B,s}$ reaches $V_{BE}(FA)$, Q_s becomes FA when

$$V_{IN} = V_{BE,s}(FA) - V_{CE,I}(sat) = V_{IL}$$

* with Q_s conducting current V_{out} begins to drop as V_{IN} increases because of the increasing voltage across R_c

Input breakpoint voltage $\equiv V_{IS}$

* As V_{IN} is increased further, since $I_{E,s} \approx I_{C,s} = I_{RD}$ the voltage at the base of Q_o begins to rise until Q_o becomes FA when

$$\begin{aligned} V_{IN} &= V_{BE,o}(FA) + V_{BE,s}(FA) - V_{CE,I}(sat) \\ &= 2V_{BE}(FA) - V_{CE}(sat) = V_{IS} \end{aligned}$$

* Note that Q_o turning on causes a change in slope of the VTC at $V_{IN} = V_{IS}$

Output breakpoint voltage $\equiv V_{OS}$

* The output voltage corresponding to V_{IS} can be found by noting that as Q_o just turns on

$$I_{RC} = I_{RD} = \frac{V_{BE,o}(FA)}{R_D}$$

Thus,

$$\begin{aligned} V_{out} &= V_{CC} - I_{RC}R_c - V_{BE,p}(FA) - V_{D_L}(ON) \\ &= V_{CC} - \left(\frac{R_c}{R_D} + 1\right)V_{BE}(FA) - V_D(ON) = V_{OS} \end{aligned}$$

Input high voltage $\equiv V_{IH}$

* Q_o & Q_s both saturate when

$$\begin{aligned} V_{IN} &= V_{BE,o}(sat) + V_{BE,s}(sat) - V_{CE,I}(sat) \\ &= 2V_{BE}(sat) - V_{CE}(sat) = V_{IH} \end{aligned}$$

Output low voltage $\equiv V_{OL}$

* with Q_o operating in saturation

$$V_{out} = V_{CE,o}(sat) = V_{OL}$$

Q_p is then turned off

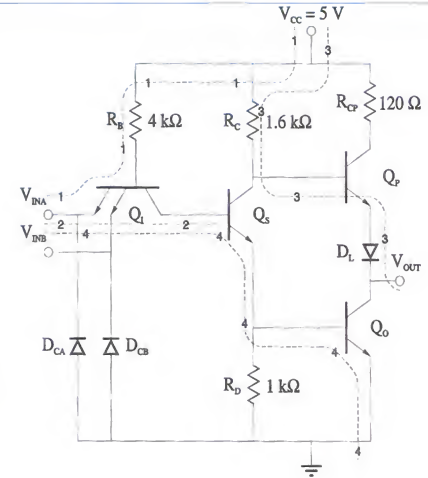


FIGURE 7.3 Standard 5400/7400 Series TTL NAND Gate with Totem-pole Output

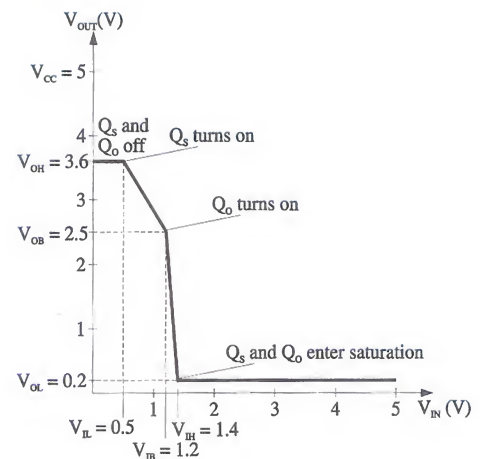


FIGURE 7.4 Voltage Transfer Characteristic for the Standard 5400/7400 Series TTL Gate

TABLE 7.2 States of Diodes and BJTs for Break-points

Element	V_{OH}	V_B	V_{OL}
Q_i	Saturated	Saturated	Reverse active
Q_s	Cutoff	Forward active	Saturated
Q_p	EOC	Forward active	Cutoff
D_i	EOC	EOC	Cutoff
Q_o	Cutoff	Edge of conduction	Saturated

Example 7.2 TTL Voltage Transfer Characteristic

Calculate V_{OH} , V_{IL} , V_{IH} , and V_{OL} as well as V_{IB} and V_{OB} for the standard TTL gate of Figure 7.3. Let $\beta_F = 100$.

$$V_{OH} = V_{CC} - V_{BE}(FA) - V_D(ON) = 5 - 0.7 - 0.7 = 3.6V$$

$$V_{IL} = V_{BE}(FA) - V_{CE}(sat) = 0.7 - 0.2 = 0.5V$$

$$V_{IB} = 2V_{BE}(FA) - V_{CE}(sat) = 2(0.7) - 0.2 = 1.2V$$

$$V_{OB} = V_{CC} - \left(\frac{R_C}{R_D}\right) V_{BE}(FA) - V_{BE}(FA) - V_D(ON)$$

$$= 5 - \left(\frac{1.6K}{1K}\right) 0.7 - 0.7 - 0.7 = 2.48V$$

$$V_{IH} = 2V_{BE}(sat) - V_{CE}(sat) = 2(0.8) - 0.2 = 1.4V$$

$$V_{OL} = V_{CE}(sat) = 0.2V$$

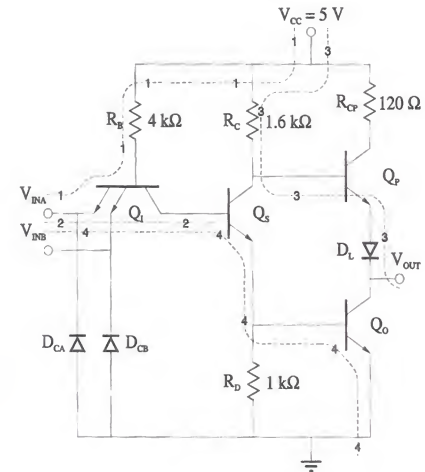


FIGURE 7.3 Standard 5400/7400 Series TTL NAND Gate with Totem-pole Output

TTL Fan-out

* The maximum fan-out for TTL is dependent on the output low state of the driver gate.

$$N = \frac{I_{OL}}{I_{IL}}$$

* In the circuit to the right $V_{out} = V_{OL} = V_{OL}$ is used for the fan-out analysis.

Input low current $\equiv I_{IL}$

* The input current of TTL gate is the emitter current of Q_1 . For the input low state (output high state) Q_1 is saturated & Q_2 is cutoff.

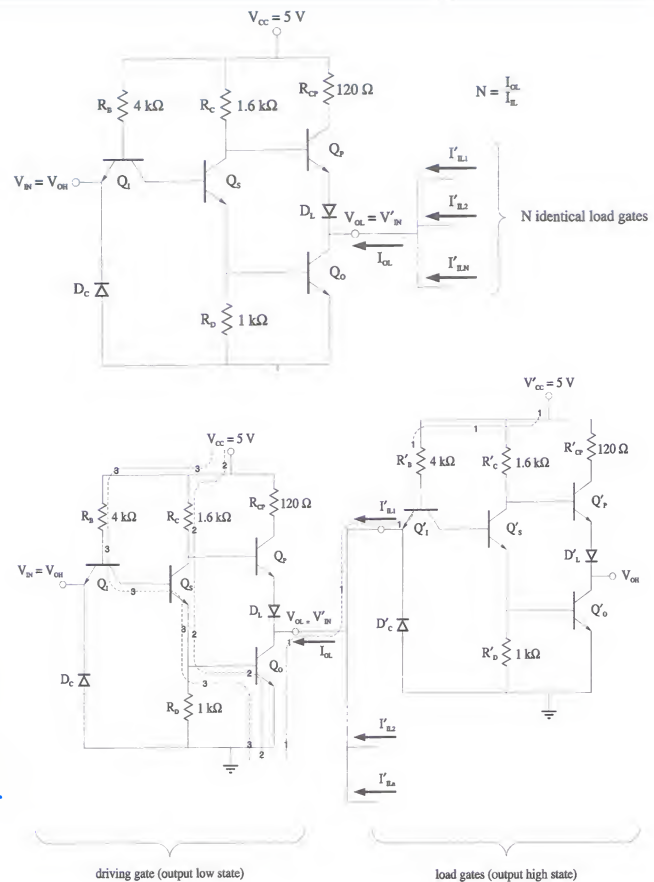


FIGURE 7.6 Cascaded TTL Gates for Fan-out and Average Power Dissipation Calculations

* Since $I_{C,I} = -I_{B,S}$, $I_{C,I}$ is essentially zero for the input low state. The input low current is then just the current in R'_B .

$$I_{IL} = \frac{V_{CC} - V_{BE,I(sat)} - V_{CE,O(sat)}}{R'_B}$$

Output Low current

* Since Q_L is cutoff for the output low state

$$I_{OL} = I_{C,O(sat)} = \sigma_{OL} \beta_F I_{B,O}$$

$$I_{B,O} = I_{E,S(sat)} - I_{R,D}$$

$$I_{R,D} = \frac{V_{BE,O(sat)}}{R_D}$$

$$I_{E,S(sat)} = I_{B,S} + I_{C,S}$$

$$I_{C,S} = I_{R,C}$$

$$= \frac{V_{CC} - V_{CE,S(sat)} - V_{BE,O(sat)}}{R_C}$$

$$I_{B,S} = I_{C,I} (R_A) = (1 + \beta_R) I_{B,I}$$

$$= (1 + \beta_R) I_{R,B}$$

$$I_{B,I} = \frac{V_{CC} - V_{CE,I} (R_A) - V_{BE,S(sat)} - V_{BE,O(sat)}}{R_B}$$

Example 7.3 TTL Fan-Out

Calculate the fan-out for the standard TTL inverter of Figure 7.5 considering the circuit of Figure 7.6 where needed. For the output low state let $\beta_F = 25$, $\beta_R = 0.1$, and $\sigma_{OL} = 0.85$. Also use $V_{BE(FA)} = V_{BE(RA)} = 0.7$ V, $V_{BE(SAT)} = 0.8$ V, and $V_{CE(SAT)} = 0.2$ V.

$$N = \frac{I_{OL}}{I_{IL}}$$

$$I_{IL} = \frac{V_{CC} - V_{BE(sat)} - V_{CE(sat)}}{R_B} = \frac{5 - 0.8 - 0.2}{4k} = 1mA$$

$$I_{OL} = I_{C,O(sat)} = \sigma_{OL} \beta_F I_{B,O}$$

$$I_{B,O} = I_{E,S(sat)} - I_{R,D}$$

$$I_{R,D} = \frac{V_{BE(sat)}}{R_D} = \frac{0.8}{1k} = 800\mu A$$

$$I_{E,S(sat)} = I_{B,S} + I_{C,S}$$

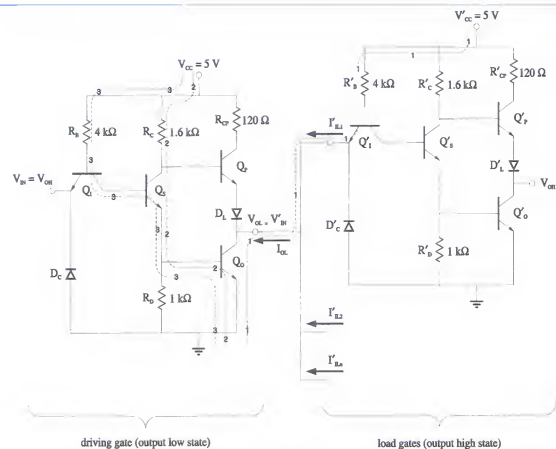


FIGURE 7.6 Cascaded TTL Gates for Fan-out and Average Power Dissipation Calculations

$$I_{C,s} = I_{RC} = \frac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{R_C} = \frac{5 - 0.8 - 0.2}{1.6k} = 2.5 \text{ mA}$$

$$I_{B,s} = I_{Q,I}(RA) = (1 + \beta_R) I_{B,I} = (1 + \beta_R) I_{RB}$$

$$I_{RB} = \frac{V_{CC} - V_{CC}(RA) - 2V_{BE(sat)}}{R_B} = \frac{5 - 0.7 - 2(0.8)}{4k} = 675 \mu\text{A}$$

$$I_{B,s} = (1 + 0.1)(675 \mu\text{A}) = 743 \mu\text{A}$$

$$I_{E,s} = 743 \mu\text{A} + 2.5 \text{ mA} = 3.24 \text{ mA}$$

$$I_{B,o} = (3.24 \text{ mA}) - (800 \mu\text{A}) = 2.44 \text{ mA}$$

$$I_{O,L} = (0.85)(25)(2.44 \text{ mA}) = 51.9 \text{ mA}$$

$$N = \frac{I_{O,L}}{I_{IL}} = \frac{51.9 \text{ mA}}{1 \text{ mA}} = 51.9$$

* The maximum fan-out of this TTL gate is 51.

TTL power dissipation

Output high current supplied $\equiv I_{CC(OH)}$

* For the output high state (the input is low with $V_{IN} = V_{CE(sat)}$)

$$I_{CC(OH)} = I_{RB(OH)}$$

$$= \frac{V_{CC} - V_{BE,I(sat)} - V_{CEQ(sat)}}{R_B}$$

Output low current supplied $\equiv I_{CC(OL)}$

* For the output low state (the input is high)

$$I_{CC(OL)} = I_{RB(OL)} + I_{RC(OL)} + I_{RCP(OL)}$$

$$I_{RB(OL)} = \frac{V_{CC} - V_{BC(RA)} - 2V_{BE(sat)}}{R_B}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{R_C}$$

$I_{RCP} = 0$ because Q_P is cutoff for the output low case

$$I_{CC(OL)} = I_{RB(OL)} + I_{RC(OL)}$$

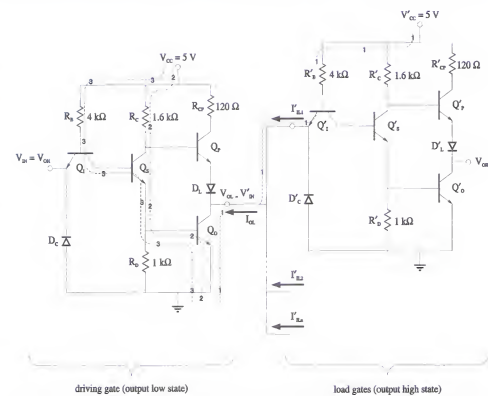


FIGURE 7.6 Cascaded TTL Gates for Fan-out and Average Power Dissipation Calculations

Average power dissipation $\equiv P_{cc(avg)}$

$$P_{cc(avg)} = \frac{I_{cc(OH)} + I_{cc(OL)}}{2} V_{cc}$$

$$= \frac{I_{RB(OH)} + I_{RB(OL)} + I_{RC(OL)}}{2} V_{cc}$$

Example 7.4 TTL Power Dissipation

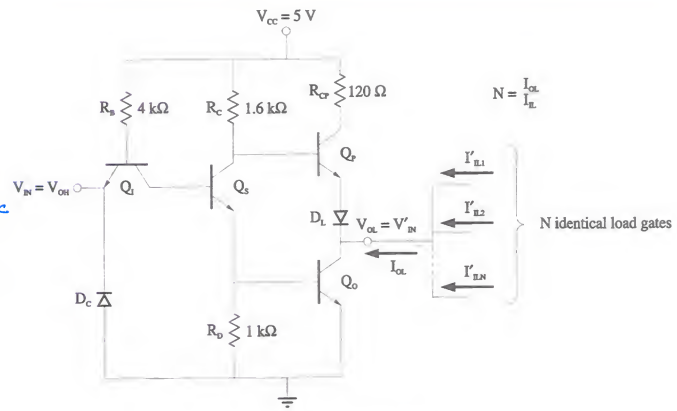
Calculate the power dissipation of the standard TTL inverter of Figure 7.5.

$$P_{cc(avg)} = \frac{I_{cc(OH)} + I_{cc(OL)}}{2} V_{cc}$$

$$= \left(\frac{I_{RB(OH)} + I_{RB(OL)} + I_{RC(OL)}}{2} \right) V_{cc}$$

$$= \frac{1m + 675\mu + 2.5m}{2} (5)$$

$$= 10.4 \text{ mW}$$



Open-collector TTL

- * These gates do not include the output-high pull-up driver made up of Q_p , D_c & R_p
- * These gates are indicated in data sheets by specifying "open-collector" or "OC"
- * Open-collector TTL gates are often used in data busses where multiple gate outputs must be ANDed. This can be accomplished by using a single pull-up resistor with open-collector TTL gates. This type of connection is referred to as a wired-AND because the output is high only when Q_o of all wired gates are cutoff.

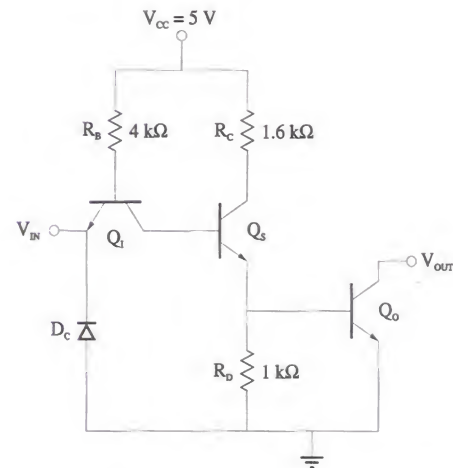


FIGURE 7.7 Open-collector TTL Gate

Low Power TTL (LTTL)

- * To decrease the power dissipated in TTL logic gates the resistor magnitudes must be increased.
- * with increased resistances less current conducts in the gate and the $I_{cc} \times V_{cc}$ product is decreased
- * The resistors are approximately one order of magnitude larger than those for the 5400/7400 Standard TTL gate
- * Disadvantages:
 - ① decreased fan-out
 - ② longer transient response times

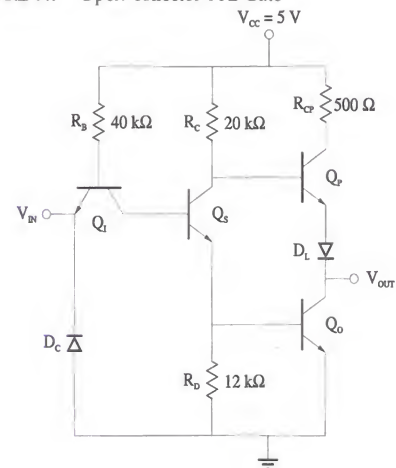


FIGURE 7.8 54L00/74L00 Low Power TTL (LTTL) with Increased Resistances

* These disadvantages result from decreased currents which sink load gate input currents & charge load capacitances. Thus, a tradeoff exists between lower power dissipation & transient response.

Example 7.5 Power Dissipation Comparison of TTL and LTTL

Compare the power dissipation for LTTL in Figure 7.8 with that of TTL found in Example 7.4. Use the BJT terminal voltages of Example 7.4.

$$P_{cc}(avg) = \frac{I_{cc}(OH) + I_{cc}(OL)}{2} V_{cc}$$

$$= \frac{I_{RB}(OH) + I_{RB}(OL) + I_{RC}(OL)}{2} V_{cc}$$

$$I_{RB}(OH) = \frac{V_{cc} - V_{BE1}(sat) - V_{CEQ}(sat)}{R_B} = \frac{5 - 0.8 - 0.2}{40k} = 100 \mu A$$

$$I_{RB}(OL) = \frac{V_{cc} - V_{BC}(RA) - 2V_{BE}(sat)}{R_B}$$

$$= \frac{5 - 0.7 - 2(0.8)}{40k} = 67.5 \mu A$$

$$I_{RC}(OL) = \frac{V_{cc} - V_{CE}(sat) - V_{BE}(sat)}{R_C} = \frac{5 - 0.2 - 0.8}{20k} = 200 \mu A$$

$$P_{cc}(avg) = \frac{(67.5 \mu A) + (200 \mu A) + (100 \mu A)}{2} (5) = 919 \mu W$$

* Comparing with example 7.4 ($P_{cc}(avg) = 10.4 mW$) we see that the power dissipation for the LTTL gate is about one tenth of that for TTL

High Speed TTL (HTTL)

* The transient response of TTL might be improved by decreasing resistance values and increasing the power dissipation.

* In addition to the decreased resistances the output-high driver section includes a Darlington pair configuration Q_{p1} & Q_{p2} in place of the single BJT Q_p used in TTL. This allows more current to be sourced for charging of the load capacitance. R_{EP} is included as a discharge path for Q_{p2} .

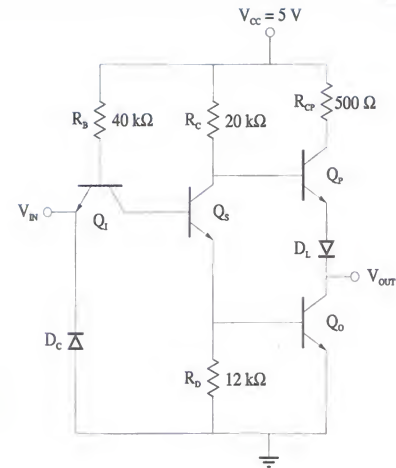


FIGURE 7.8 54L00/74L00 Low Power TTL (LTTL) with Increased Resistances

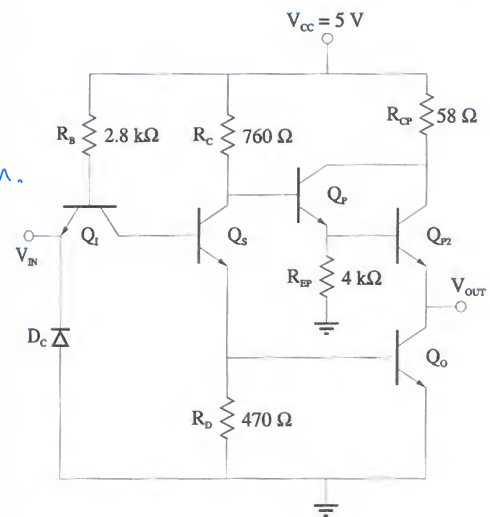


FIGURE 7.9 54H00/74H00 High Speed TTL (HTTL) with Smaller Resistances and Darlington Pair Output High Driver

TTL SPICE simulation

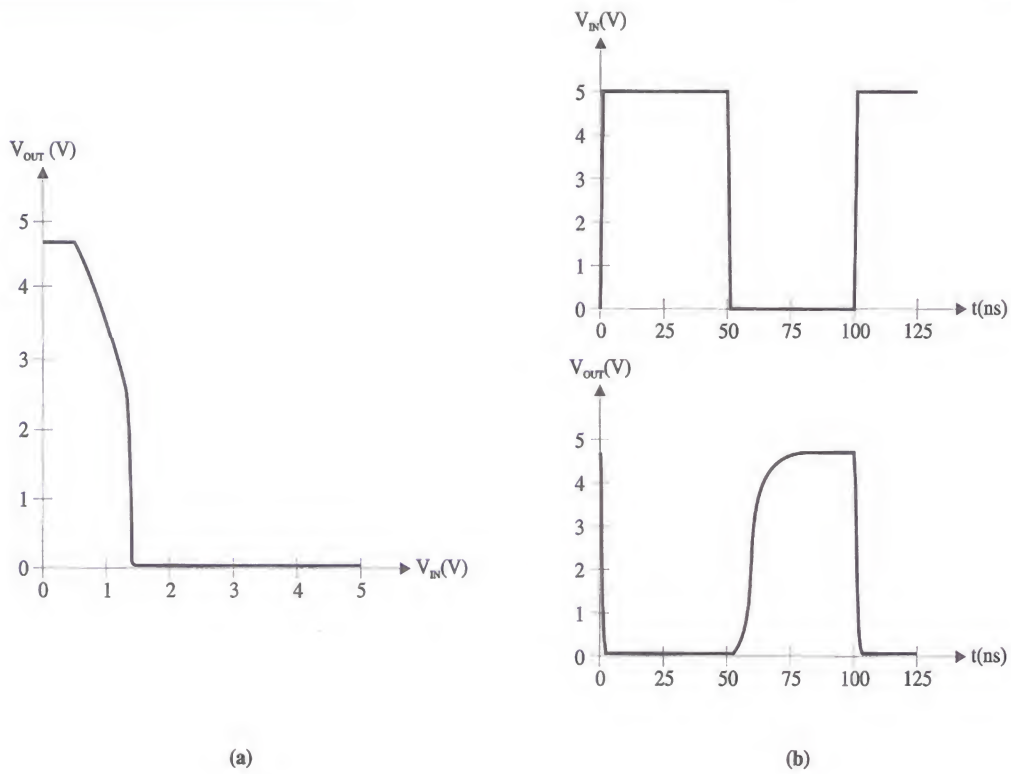
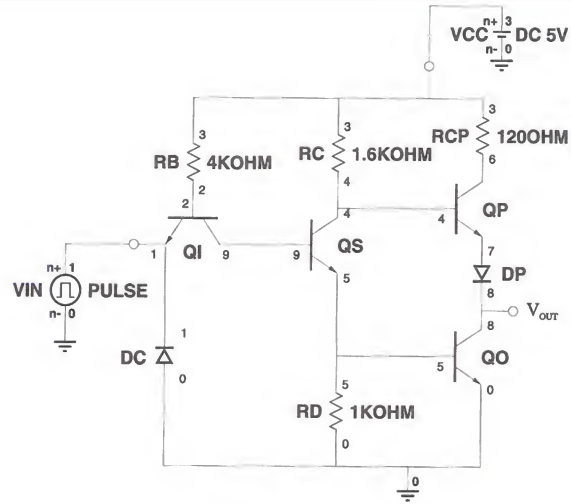


FIGURE 7.11 Results of Section 7.11 TTL SPICE Simulation: (a) Voltage transfer characteristic from .DC

sweep, (b) Transient response from .TRAN sweep

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